SPECIFICATION AMENDMENTS

At page 1, lines 1-2, please amend the Title as follows:

~~MICROPROCESSOR WITH HARDWARE CONTROLLED POWER MANAGEMENT~~ PIPELINED DATA PROCESSOR WITH INSTRUCTION-INITIATED POWER MANAGEMENT CONTROL

At page 1, between lines 2 and 3, please insert the following:

RELATED APPLICATIONS

This is a division of U.S. patent application no. 10/216,615, filed August 9, 2002.

At page 1, lines 4-6, please amend the text of the section entitled "Technical Field of the Invention" as follows:

This invention relates in general to integrated circuits, and more particularly to a ~~microprocessor having hardware controlled~~ pipelined data processor with power management control.

At page 4, lines 3-21, please amend the text of the section entitled "Summary of the Invention" as follows:

~~In accordance with the present invention, a method and apparatus is provided which provides significant advantages in reducing the power consumption of a microprocessor.~~

~~In the present invention, a processing unit includes a plurality of subcircuits and circuitry for generating a clock signal thereto. Circuitry is provided for detecting the assertion of a control signal; responsive to the control signal, disabling circuitry disables the clock signal to one or more of the subcircuits.~~

~~The present invention provides significant advantages over the prior art. A significant reduction in the power consumed by a computer may be effected by disabling the clock to the microprocessor circuitry. The present invention allows the disabling and enabling of the microprocessor clock signals to be controlled by a single control signal. Further, an acknowledge signal may be provided to notify external circuitry of the suspended state of the microprocessor.~~

In accordance with the presently claimed invention, a pipelined data processor with instruction-initiated power management control is provided in which a plurality of subcircuits, including pipeline subcircuitry, and circuitry for generating and controlling at least one clock signal are responsive to an instruction executed by the pipeline subcircuitry by selectively disabling a clock signal to the pipeline subcircuitry.

In accordance with one embodiment of the presently claimed invention, an apparatus including integrated processor circuitry includes a plurality of interface electrodes, a plurality of subcircuits, control circuitry and clock circuitry. The plurality of interface electrodes conveys at least a plurality of incoming instructions, including a power management instruction, from at least one signal source. The plurality of subcircuits is coupled to at least a portion of the plurality of interface electrodes and includes pipeline subcircuitry responsive to a first clock signal having active and inactive states by selectively operating on one or more of the plurality of incoming instructions for data processing. A first portion of the pipeline subcircuitry is responsive to the active first clock signal by performing at least one or more respective portions of one or more processing, including decoding, operations upon at least one or more respective portions of the one or more of the plurality of incoming instructions to provide one or more decoded instructions and to provide one or more local control signals having one or more respective assertion and de-assertion states including one or more first selected assertion and de-assertion states corresponding to the power management instruction, and a second portion of the pipeline subcircuitry is coupled to the first pipeline subcircuitry portion and responsive to the active first

clock signal by executing the one or more decoded instructions. The control circuitry is coupled to the plurality of subcircuits and responsive to the one or more local control signals by providing one or more clock control signals having one or more respective assertion and de-assertion states including one or more second selected assertion and de-assertion states corresponding to the one or more first selected assertion and de-assertion states of the one or more local control signals with the second selected assertion and de-assertion states following reception of the power management instruction. The clock circuitry is coupled to the control circuitry and the plurality of subcircuits, and responsive to the one or more clock control signals by providing at least the first clock signal with the first clock signal inactive state corresponding to the one or more second selected assertion and de-assertion states of the one or more clock control signals.

In accordance with another embodiment of the presently claimed invention, an apparatus including integrated processor circuitry includes interface means, subcircuit means, controller means and clock source means. The interface means is for conveying at least a plurality of incoming instructions, including a power management instruction, from at least one signal source. The subcircuit means includes pipeline means for responding to a first clock signal having active and inactive states by selectively operating on one or more of the plurality of incoming instructions for data processing. A first portion of the pipeline means is for responding to the active first clock signal by performing at least one or more respective portions of one or more processing, including decoding, operations upon at least one or more respective portions of the one or more of the plurality of incoming instructions to provide one or more decoded instructions and to provide one or more local control signals having one or more respective assertion and de-assertion states including one or more first selected assertion and de-assertion states corresponding to the power management instruction, and a second portion of the pipeline means is for responding to the active first clock signal by executing the one or more decoded instructions. The controller means is for responding to the one or more local control

signals by generating one or more clock control signals having one or more respective assertion and de-assertion states including one or more second selected assertion and de-assertion states corresponding to the one or more first selected assertion and de-assertion states of the one or more local control signals with the second selected assertion and de-assertion states following reception of the power management instruction. The clock source means is for responding to the one or more clock control signals by generating at least the first clock signal with the first clock signal inactive state corresponding to the one or more second selected assertion and de-assertion states of the one or more clock control signals.

In accordance with another embodiment of the presently claimed invention, an apparatus including integrated processor circuitry includes a plurality of interface electrodes, a plurality of subcircuits, control circuitry and clock circuitry. The plurality of interface electrodes conveys at least a plurality of incoming instructions, including a power management instruction, from at least one signal source. The plurality of subcircuits coupled to at least a portion of the plurality of interface electrodes and includes pipeline subcircuitry responsive to a first clock signal having active and inactive states by selectively operating on one or more of the plurality of incoming instructions for data processing. A first portion of the pipeline subcircuitry is responsive to the active first clock signal by performing at least one or more respective portions of one or more processing, including decoding, operations upon at least one or more respective portions of the one or more of the plurality of incoming instructions to provide one or more decoded instructions and to provide one or more local control signals having one or more respective assertion and de-assertion states including one or more first selected assertion and de-assertion states corresponding to the power management instruction, and a second portion of the pipeline subcircuitry is coupled to the first pipeline subcircuitry portion and responsive to the active first clock signal by executing the one or more decoded instructions. The control circuitry is coupled to the plurality of subcircuits and responsive to the one or more local control signals by providing one or more clock control signals having one or more

respective assertion and de-assertion states including one or more second selected assertion and de-assertion states corresponding to the one or more first selected assertion and de-assertion states of the one or more local control signals. The clock circuitry is coupled to the control circuitry and the plurality of subcircuits, and responsive to the one or more clock control signals by providing at least the first clock signal with the first clock signal inactive state corresponding to the one or more second selected assertion and de-assertion states of the one or more clock control signals and following reception of the power management instruction.

In accordance with another embodiment of the presently claimed invention, an apparatus including integrated processor circuitry includes interface means, subcircuit means, controller means and clock source means. The interface means is for conveying at least a plurality of incoming instructions, including a power management instruction, from at least one signal source. The subcircuit means includes pipeline means for responding to a first clock signal having active and inactive states by selectively operating on one or more of the plurality of incoming instructions for data processing. A first portion of the pipeline means is for responding to the active first clock signal by performing at least one or more respective portions of one or more processing, including decoding, operations upon at least one or more respective portions of the one or more of the plurality of incoming instructions to provide one or more decoded instructions and to provide one or more local control signals having one or more respective assertion and de-assertion states including one or more first selected assertion and de-assertion states corresponding to the power management instruction, and a second portion of the pipeline means is for responding to the active first clock signal by executing the one or more decoded instructions. The controller means is for responding to the one or more local control signals by generating one or more clock control signals having one or more respective assertion and de-assertion states including one or more second selected assertion and de-assertion states corresponding to the one or more first selected assertion and de-assertion states of the one or more local control signals. The clock source means is for

responding to the one or more clock control signals by generating at least the first clock signal with the first clock signal inactive state corresponding to the one or more second selected assertion and de-assertion states of the one or more clock control signals and following reception of the power management instruction.

In accordance with another embodiment of the presently claimed invention, an apparatus including integrated processor circuitry includes a plurality of interface electrodes, a plurality of subcircuits, control circuitry and clock circuitry. The plurality of interface electrodes conveys at least a plurality of incoming instructions, including a power management instruction, from at least one signal source. The plurality of subcircuits is coupled to at least a portion of the plurality of interface electrodes and includes pipeline subcircuitry responsive to a first clock signal having an active state with a plurality of successive cycles and an inactive state with substantially zero cycles by selectively operating on one or more of the plurality of incoming instructions for data processing. A first portion of the pipeline subcircuitry is responsive to at least a first one of the plurality of first clock signal cycles by performing at least one or more respective portions of one or more processing, including decoding, operations upon at least one or more respective portions of the one or more of the plurality of incoming instructions to provide one or more decoded instructions and to provide one or more local control signals having one or more respective assertion and de-assertion states including one or more first selected assertion and de-assertion states corresponding to the power management instruction, and a second portion of the pipeline subcircuitry is coupled to the first pipeline subcircuitry portion and responsive to at least a second one subsequent to the first one of the plurality of first clock signal cycles by executing the one or more decoded instructions. The control circuitry is coupled to the plurality of subcircuits and responsive to the one or more local control signals by providing one or more clock control signals having one or more respective assertion and de-assertion states including one or more second selected assertion and de-assertion states corresponding to the one or more first selected assertion and de-assertion states of the one or more

local control signals with the second selected assertion and de-assertion states following reception of the power management instruction. The clock circuitry is coupled to the control circuitry and the plurality of subcircuits, and responsive to the one or more clock control signals by providing at least the first clock signal with the first clock signal inactive state corresponding to the one or more second selected assertion and de-assertion states of the one or more clock control signals.

In accordance with another embodiment of the presently claimed invention, an apparatus including integrated processor circuitry includes interface means, subcircuit means, controller means and clock source means. The interface means is for conveying at least a plurality of incoming instructions, including a power management instruction, from at least one signal source. The subcircuit means includes pipeline means for responding to a first clock signal having an active state with a plurality of successive cycles and an inactive state with substantially zero cycles by selectively operating on one or more of the plurality of incoming instructions for data processing. A first portion of the pipeline means is for responding to at least a first one of the plurality of first clock signal cycles by performing at least one or more respective portions of one or more processing, including decoding, operations upon at least one or more respective portions of the one or more of the plurality of incoming instructions to provide one or more decoded instructions and to provide one or more local control signals having one or more respective assertion and de-assertion states including one or more first selected assertion and de-assertion states corresponding to the power management instruction, and a second portion of the pipeline means is for responding to at least a second one subsequent to the first one of the plurality of first clock signal cycles by executing the one or more decoded instructions. The controller means is for responding to the one or more local control signals by generating one or more clock control signals having one or more respective assertion and de-assertion states including one or more second selected assertion and de-assertion states corresponding to the one or more first selected assertion and de-assertion states of the one or more local control signals with the second selected

assertion and de-assertion states following reception of the power management instruction The clock source means is for responding to the one or more clock control signals by generating at least the first clock signal with the first clock signal inactive state corresponding to the one or more second selected assertion and de-assertion states of the one or more clock control signals.

In accordance with another embodiment of the presently claimed invention, an apparatus including integrated processor circuitry includes a plurality of interface electrodes, a plurality of subcircuits, control circuitry and clock circuitry. The plurality of interface electrodes conveys at least a plurality of incoming instructions, including a power management instruction, from at least one signal source. The plurality of subcircuits is coupled to at least a portion of the plurality of interface electrodes and includes pipeline subcircuitry responsive to a first clock signal having an active state with a plurality of successive cycles and an inactive state with substantially zero cycles by selectively operating on one or more of the plurality of incoming instructions for data processing. A first portion of the pipeline subcircuitry is responsive to at least a first one of the plurality of first clock signal cycles by performing at least one or more respective portions of one or more processing, including decoding, operations upon at least one or more respective portions of the one or more of the plurality of incoming instructions to provide one or more decoded instructions and to provide one or more local control signals having one or more respective assertion and de-assertion states including one or more first selected assertion and de-assertion states corresponding to the power management instruction, and a second portion of the pipeline subcircuitry is coupled to the first pipeline subcircuitry portion and responsive to at least a second one subsequent to the first one of the plurality of first clock signal cycles by executing the one or more decoded instructions. The control circuitry is coupled to the plurality of subcircuits and responsive to the one or more local control signals by providing one or more clock control signals having one or more respective assertion and de-assertion states including one or more second selected assertion and de-assertion states corresponding

to the one or more first selected assertion and de-assertion states of the one or more local control signals. The clock circuitry is coupled to the control circuitry and the plurality of subcircuits, and responsive to the one or more clock control signals by providing at least the first clock signal with the first clock signal inactive state corresponding to the one or more second selected assertion and de-assertion states of the one or more clock control signals and following reception of the power management instruction.

In accordance with another embodiment of the presently claimed invention, an apparatus including integrated processor circuitry includes interface means, subcircuit means, controller means and clock source means. The interface means is for conveying at least a plurality of incoming instructions, including a power management instruction, from at least one signal source. The subcircuit means includes pipeline means for responding to a first clock signal having an active state with a plurality of successive cycles and an inactive state with substantially zero cycles by selectively operating on one or more of the plurality of incoming instructions for data processing. A first portion of the pipeline means is for responding to at least a first one of the plurality of first clock signal cycles by performing at least one or more respective portions of one or more processing, including decoding, operations upon at least one or more respective portions of the one or more of the plurality of incoming instructions to provide one or more decoded instructions and to provide one or more local control signals having one or more respective assertion and de-assertion states including one or more first selected assertion and de-assertion states corresponding to the power management instruction, and a second portion of the pipeline means is for responding to at least a second one subsequent to the first one of the plurality of first clock signal cycles by executing the one or more decoded instructions. The controller means is for responding to the one or more local control signals by generating one or more clock control signals having one or more respective assertion and de-assertion states including one or more second selected assertion and de-assertion states corresponding to the one or more first

selected assertion and de-assertion states of the one or more local control signals. The clock source means is for responding to the one or more clock control signals by generating at least the first clock signal with the first clock signal inactive state corresponding to the one or more second selected assertion and de-assertion states of the one or more clock control signals and following reception of the power management instruction.

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one or more local control signals with the second selected assertion and de-assertion states following reception of the power management instruction. The clock circuitry is coupled to the control circuitry and the plurality of subcircuits, and responsive to the one or more clock control signals by providing the first and second clock signals with the first clock signal inactive state corresponding to the one or more second selected assertion and de-assertion states of the one or more clock control signals and the second clock signal having active and inactive states substantially independent of the one or more second selected assertion and de-assertion states of the one or more clock control signals.

In accordance with another embodiment of the presently claimed invention, an apparatus including integrated processor circuitry includes interface means, subcircuit means, controller means and clock source means. The interface means is for conveying at least a plurality of incoming instructions, including a power management instruction, from at least one signal source. The subcircuit means includes pipeline means for responding to a first clock signal having active and inactive states by selectively operating on one or more of the plurality of incoming instructions for data processing. A first portion of the pipeline means is for responding to the active first clock signal by performing at least one or more respective portions of one or more processing, including decoding, operations upon at least one or more respective portions of the one or more of the plurality of incoming instructions to provide one or more decoded instructions and to provide one or more local control signals having one or more respective assertion and de-assertion states including one or more first selected assertion and de-assertion states corresponding to the power management instruction, and a second portion of the pipeline means is for responding to the active first clock signal by executing the one or more decoded instructions. The controller means is for responding to the first clock signal, a second clock signal and the one or more local control signals by generating one or more clock control signals having one or more respective assertion and de-assertion states including one or more second selected assertion and de-assertion states corresponding

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In accordance with another embodiment of the presently claimed invention, an apparatus including integrated processor circuitry includes a plurality of interface electrodes, a plurality of subcircuits, control circuitry and clock circuitry. The plurality of interface electrodes conveys at least a plurality of incoming instructions, including a power management instruction, from at least one signal source. The plurality of subcircuits is coupled to at least a portion of the plurality of interface electrodes and includes pipeline subcircuitry responsive to a first clock signal having active and inactive states by selectively operating on one or more of the plurality of incoming instructions for data processing. A first portion of the pipeline subcircuitry is responsive to the active first clock signal by performing at least one or more respective portions of one or more processing, including decoding, operations upon at least one or more respective portions of the one or more of the plurality of incoming instructions to provide one or more decoded instructions and to provide one or more local control signals having one or more respective assertion and de-assertion states including one or more first selected assertion and de-assertion states corresponding to the power management instruction, and a second portion of the pipeline subcircuitry is coupled to the first pipeline subcircuitry portion and responsive to the active first clock signal by executing the one or more decoded instructions. The control circuitry is coupled to the plurality of subcircuits and responsive to the first clock signal, a second clock signal and the one or more local control signals by providing one or

more clock control signals having one or more respective assertion and de-assertion states including one or more second selected assertion and de-assertion states corresponding to the one or more first selected assertion and de-assertion states of the one or more local control signals. The clock circuitry is coupled to the control circuitry and the plurality of subcircuits, and responsive to the one or more clock control signals by providing the first and second clock signals with the first clock signal inactive state corresponding to the one or more second selected assertion and de-assertion states of the one or more clock control signals and following reception of the power management instruction, and with the second clock signal having active and inactive states substantially independent of the one or more second selected assertion and de-assertion states of the one or more clock control signals.

In accordance with another embodiment of the presently claimed invention, an apparatus including integrated processor circuitry includes interface means, subcircuit means, controller means and clock source means. The interface means is for conveying at least a plurality of incoming instructions, including a power management instruction, from at least one signal source. The subcircuit means includes pipeline means for responding to a first clock signal having active and inactive states by selectively operating on one or more of the plurality of incoming instructions for data processing. A first portion of the pipeline means is for responding to the active first clock signal by performing at least one or more respective portions of one or more processing, including decoding, operations upon at least one or more respective portions of the one or more of the plurality of incoming instructions to provide one or more decoded instructions and to provide one or more local control signals having one or more respective assertion and de-assertion states including one or more first selected assertion and de-assertion states corresponding to the power management instruction, and a second portion of the pipeline means is for responding to the active first clock signal by executing the one or more decoded instructions. The controller means is for responding to the first clock signal, a second clock signal and the one or more local control signals by generating one or more clock

control signals having one or more respective assertion and de-assertion states including one or more second selected assertion and de-assertion states corresponding to the one or more first selected assertion and de-assertion states of the one or more local control signals. The clock source means is for responding to the one or more clock control signals by generating the first and second clock signals with the first clock signal inactive state corresponding to the one or more second selected assertion and de-assertion states of the one or more clock control signals and following reception of the power management instruction, and with the second clock signal having active and inactive states substantially independent of the one or more second selected assertion and de-assertion states of the one or more clock control signals.

At page 19, lines 3-8, please amend the text of the section entitled "Abstract of the Disclosure" as follows:

~~A processing unit includes a plurality of subcircuits and circuitry for generating clock signals thereto. Detection circuitry detects the assertion of a control signal and disabling circuitry is operable to disable the clock signals to one or more of the subcircuits responsive to the control signal.~~ A pipelined data processor with instruction-initiated power management control in which a plurality of subcircuits, including pipeline subcircuitry, and circuitry for generating and controlling at least one clock signal are responsive to an instruction executed by the pipeline subcircuitry by selectively disabling a clock signal to the pipeline subcircuitry.